PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10056373	01/17/2002	250	214R	2878	R. Ellis

**APPLICANTS: Bretschneider Ernst; Fuhrmann Johann; Einfeldt Walter;

**CONTINUING DATA VERIFIED:

None

** FOREIGN APPLICATIONS VERIFIED:

GERMANY 10101995.5 01/18/2001 TMR

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO.
35 USC 119 conditions met	☐ yes ☐ no		DE 010005
Verified and Acknowledged Examiners's intials			

TITLE : Circuit arrangement and method of protecting at least a chip arrangement from manipulation and/or abuse

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
	Assistant Examiner	Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs Drwg. / Print Fig	
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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